WHAT IS CLAIMED IS:

1. A circuit for prevention of unintentional writing to a memory, comprising:

a detection circuit that detects a drop in power supply voltage and outputs a first reset signal in response thereto, said detection circuit being capable of being turned on and off by a control signal from a control terminal; and

a control signal detecting circuit that detects a change in said control signal and outputs a second reset signal in response thereto;

wherein a data input or output operation to said memory is prohibited in response to either said first reset signal or said second reset signal.

2. The circuit for prevention of unintentional writing to a memory as recited in claim 1, wherein said memory is a nonvolatile memory which requires a voltage above a certain level at the time of writing.

3. The circuit for prevention of unintentional writing to a memory as recited in claim 1, further comprising a register which registers and outputs the control signal,

wherein said register turns on said detection circuit upon a drop in power supply voltage when said register is in a first state, and

wherein a data input or output operation to said memory is prohibited by said control signal detecting circuit upon a drop in power supply voltage when said register is in a second state.

4. The circuit for prevention of unintentional writing to a memory as recited in claim 3, further comprising a first inverter connected between said register and said detection circuit and a second inverter to which said control signal of said register is to be inputted, said second inverter being part of said control signal detecting circuit,

wherein said first inverter and said second inverter have different threshold levels for determining ON/OFF states thereof.

5. The circuit for prevention of unintentional writing to a memory as recited in claim 4, further comprising a mode control register that controls operating status of said memory, said mode control register being resettable by either said first reset signal or said second reset signal.

6. The circuit for prevention of unintentional writing to a memory as recited in claim 5, further comprising a read/write controller that outputs a read-enable signal, a write-enable signal and an address signal and also performs inputting/outputting of data to said memory based on an output signal of said mode control register.

7. The circuit for prevention of unintentional writing to a memory as recited in claim 6, wherein said memory is a nonvolatile memory which requires a voltage above a certain level at the time of writing.

8. A circuit for prevention of unintentional writing to a memory, comprising:

a mode control register that controls data input/output operating states of said memory, said mode control register being resettable by a reset signal;

a low-voltage detection circuit that detects a drop in power supply voltage and outputs a first reset signal to reset said mode control register, said low-voltage detection circuit being turned on and off by a standby control signal from a standby control register; and

a standby control signal detecting circuit that detects a change in said standby control signal and outputs an operation prohibition signal to said mode control register to prevent a data input or output operation to said memory when said low-voltage detection circuit is turned off at the time of said drop in power supply voltage.

9. The circuit for prevention of unintentional writing to a memory as recited in claim 8, wherein said memory is a nonvolatile memory which requires a voltage above a certain level at the time of writing.

10. The circuit for prevention of unintentional writing to a memory as recited in claim 8, further comprising a first inverter connected between said standby control register and said low-voltage detection circuit and a second inverter to which said operation prohibition signal is to be inputted, said second inverter being part of said standby control signal detecting circuit,

wherein said first inverter and said second inverter have different threshold levels for determining ON/OFF states thereof.

11. The circuit for prevention of unintentional writing to a memory as recited in claim 8, further comprising a writing/reading controller that outputs a read-enable signal, a write-enable signal and an address signal and also performs inputting/outputting of data to said memory based on an output signal of said mode control register.

12. The circuit for prevention of unintentional writing to a memory as recited in claim 8, further comprising:

a first inverter connected between said standby control register and said low-voltage detection circuit and a second inverter to which said operation prohibition signal is to be inputted, said second inverter being part of said standby control signal detecting circuit, and said first inverter and said second inverter having different threshold levels for determining ON/OFF states thereof; and

a writing/reading controller that outputs a read-enable signal, a write-enable signal and an address signal and also performs inputting/outputting of data to said memory based on an output signal of said mode control register,

wherein said memory is a nonvolatile memory which requires a voltage above a certain level at the time of writing.

13. A semiconductor device equipped with said circuit for prevention of unintentional writing to said memory as recited in claim 1.

14. The semiconductor device equipped with said circuit for prevention of unintentional writing to said memory as recited in claim 13, further comprising a microcomputer,

wherein said microcomputer, said detection circuit, said control signal detecting circuit and said memory are integrally formed as a single chip on a semiconductor substrate.

15. A circuit for preventing unintentional writing to a memory, comprising:

a memory that is capable of receiving data to be stored in a writing operation, and of outputting stored data in a reading operation;

a memory operation mode controller for controlling an operational mode of said memory, said memory operation mode controller being resettable to a default state in response to receipt of a reset signal; and

a low-voltage detection circuit for detecting a drop in voltage level of a power supply voltage, and for outputting the reset signal to said memory operation mode controller in response to detection of said drop in voltage.

16. The circuit for prevention of unintentional writing to a memory as recited in claim 15, wherein said memory is a nonvolatile memory which requires a voltage above a certain level at the time of writing.

17. The circuit for prevention of unintentional writing to a memory as recited in claim 15, wherein said low-voltage detection circuit is capable of being turned on and off by a control signal from a control terminal.

18. The circuit for prevention of unintentional writing to a memory as recited in claim 15, wherein said memory operation mode controller includes a mode control register that controls operating status of said memory, said mode control register being resettable by said reset signal, and a writing/reading controller that outputs a read-enable signal, a write-enable signal and an address signal and also performs inputting/outputting of data to said memory based on an output signal of said mode control register.

19. The circuit for prevention of unintentional writing to a memory as recited in claim 15, wherein said memory is a nonvolatile memory which requires a voltage above a certain level at the time of writing.

20. A non-volatile memory system, comprising:

a non-volatile memory for storing data received in a writing operation, and for reading out stored data in a reading operation;

a mode control register for controlling an operational mode of said non-volatile memory to enable data writing or data reading operations;

a low-voltage detection circuit that detects a drop in power supply voltage level, and outputs a reset signal to said mode control register to reset an operational mode of said non-volatile memory when a drop in power supply voltage has been detected, said low-voltage detection circuit being turned on and off by a control signal from a standby control terminal;

a writing prevention circuit that prevents said mode control register from enabling a writing operation to said non-volatile memory when a drop in power supply voltage occurs while said low-voltage detection circuit is turned off.